Microwave Phase Detectors for PSK Demodulators

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Abstract—**The simplest circuits for microwave phase detectors and their operation are described. Approximate analytical expressions for the output characteristic of the various circuits are given. Accurate prediction of detector performance is achieved with a large-signal nonlinear analysis using simultaneously the time- and frequency-domain approach.**

Applying the theory developed, the effects which cause deformation of the detector characteristic are investigated. Results of practical circuits operating in the 14-GHz range are given and compared with regard to phase-demodulator applications. A low-level phase detector is presented which permits 20-dB level variation with less than 2° phase error.

I. Introduction

PHASE DETECTORS are widely used in phase demodulators, phase-locked loops, and phase-measuring equipment. In these applications, phase detection is usually performed at relatively low frequencies, and frequently after downconversion of the original high-frequency signal. Phase detection directly performed at microwave frequencies would, in many cases, lead to a reduction in hardware complexity. This is of particular interest for future communication systems using digital transmission in connection with phase-shift keying (PSK).

Up to now, there has been lack of literature on microwave phase detectors. The only papers existing particularly on this subject [1], [2] are from one author. In these papers, phase detection is considered as a mixing process, which eventually leads to some false conclusions.

The present paper describes the simplest circuits for microwave phase detectors and their principle of operation. It is shown that phase detection should be considered as peak detection rather than as a mixing process. Using simplified assumptions, analytical expressions for the output characteristic of phase detectors are derived. In order to investigate phase detectors theoretically in more detail, an accurate nonlinear analysis has been applied.

The computer-aided numerical analysis is carried out using simultaneously the time-domain and the frequency-domain approach. For this purpose, the circuit is divided into a linear and a nonlinear part. The linear part consisting of the driving-signal sources, a transmission-line network, and the linear elements of the diode equivalent circuit is treated in the frequency domain, whereas the remaining nonlinear diode elements are treated in the time domain. The solution is obtained iteratively by matching the voltage waveforms at the boundaries between the linear and the nonlinear circuit parts.

Using the analytical expressions and the nonlinear analysis, the origins of deviations from the ideal detector characteristic are investigated. The results show the crucial points in phase-detector design.

Finally, experimental results of two different detector circuits are given and compared to the theory developed here. The circuits are also compared with respect to their practical application in PSK demodulators.

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II. Simple Detector Circuits and their Operation

A phase detector compares the phases of two periodic signals of the same frequency and delivers a voltage which is a measure of the phase difference between the signals. This function is accomplished by transferring the phase difference into an amplitude difference or variation and measuring the amplitude by peak detection. Any mixer with a dc-coupled output port performs this function, however, the output characteristics obtained can be quite different.

Fig. 1 shows the three simplest circuits for phase detectors. In circuit (a), the two signals are simply added and rectified. Under the assumption of an ideal diode and a properly chosen RC network, the output voltage V_O is equal to the peak value of the RF voltage V_D applied to the diode. Thus the output voltage is given by

$$V_O = \sqrt{2\left(|V_{I1}|^2 + 2|V_{I1}||V_{I2}|\cos\varphi + |V_{I2}|^2\right)} \qquad (1)$$

where V_{I1} and V_{I2} denote the phasors of the input voltages and φ their phase difference. If the input signals are of the same amplitude $|V_{I1}| = |V_{I2}| = |V_I|$, (1) reduces to

$$V_O = 2\sqrt{2}\,|V_I|\left|\cos\left(\frac{\varphi}{2}\right)\right| \qquad (2)$$

which leads to the detector characteristic shown in Fig. 1(a). Since circuit (a) delivers only a voltage of one polarity and reaches a zero voltage solely with equal input amplitudes it is unsuitable for most phase detector applications.

Circuit (b) in Fig. 1 uses two diodes, and the difference of the rectified voltages is taken for the output. Before rectification, the signals are superimposed in a 3-dB hy-

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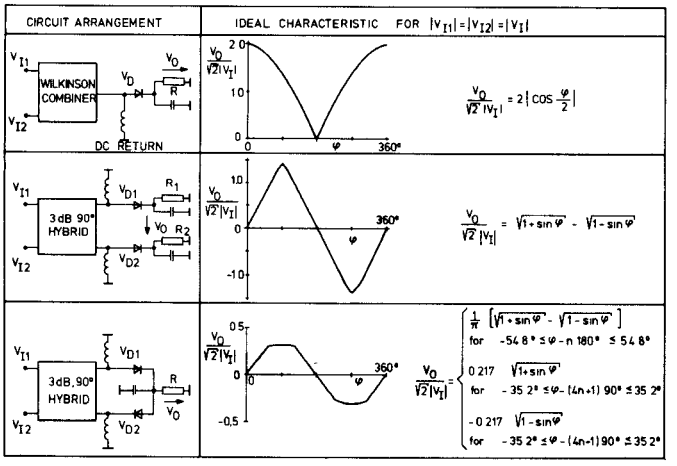

Fig. 1. Phase detector circuits and their ideal characteristic for equal input amplitudes.

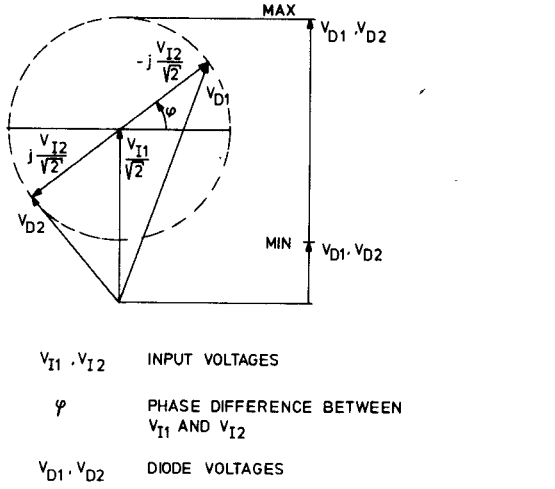

Fig. 2. Vector diagram of phase detector with 90° hybrid coupler.

brid. In case of a 90° hybrid, the RF voltages of the diodes become

$$V_{D1}=1/\sqrt{2}\,(V_{I1}-jV_{I2})$$
$$V_{D2}=1/\sqrt{2}\,(-jV_{I1}+V_{I2}) \tag{3}$$

where an ideal circuit and matched diodes are assumed. Fig. 2 illustrates how the hybrid transfers the phase difference between the input signals into an amplitude difference between the diode voltages. Assuming ideal peak detection, the output voltage $V_O=\sqrt{2}\,(|V_{D1}|-|V_{D2}|)$ is obtained from (3) as

$$V_O=\sqrt{|V_{I1}|^2+|V_{I2}|^2+2|V_{I1}||V_{I2}|\sin\varphi}$$
$$-\sqrt{|V_{I1}|^2+|V_{I2}|^2-2|V_{I1}||V_{I2}|\sin\varphi}\,. \tag{4}$$

For equal input amplitudes $|V_{I1}|=|V_{I2}|=|V_I|$, (4) reduces to

$$V_O=\sqrt{2}\,|V_I|\left(\sqrt{(1+\sin\varphi)}-\sqrt{(1-\sin\varphi)}\right). \tag{5}$$

This detector characteristic is also shown in Fig. 1. The sharp peaks of the response at $\varphi=\pi/2$ and $\varphi=3\pi/2$ are rounded if a difference occurs between the input amplitudes. If one input signal strongly dominates, e.g., $|V_{I2}|\gg|V_{I1}|$, (4) can be approximated by

$$V_O=2|V_{I1}|\sin\varphi. \tag{6}$$

The sinusoidal response (6), which is also given in [3], is often referred to as the ideal phase detector characteristic. It should be emphasized, however, that the sinusoidal characteristic is only obtained for a large-level difference at the input.

Circuit (c) in Fig. 1 is commonly used for single balanced mixers. In contrast to circuit (b), the output voltage is not simply given by the difference between the diode voltages, since, at any phase angle, one of the diodes temporarily discharges the capacitor. Assuming that the current in the output resistor $I_O=V_O/R$ is negligible compared to the diode currents, one can obtain implicit transcendental equations between V_O, V_{D1}, and V_{D2}. These equations are well approximated by

$$V_O=\frac{\sqrt{2}}{\pi}(|V_{D1}|-|V_{D2}|),\qquad \text{for } 0.318\leqslant\frac{|V_{D1}|}{|V_{D2}|}\leqslant 3.149 \tag{7}$$

and

$$V_0=0.217\sqrt{2}\begin{cases}|V_{D1}|, & \text{for } |V_{D2}|\leqslant 0.318|V_{D1}|\\ -|V_{D2}|, & |V_{D1}|\leqslant 0.318|V_{D2}|.\end{cases} \tag{8}$$

Using (3), the response of circuit (c) can be calculated from (7) and (8).

For equal input amplitudes $|V_{I1}|=|V_{I2}|=|V_I|$, the equations simplify to

$$V_O=\frac{\sqrt{2}\,|V_I|}{\pi}\left(\sqrt{1+\sin\varphi}-\sqrt{1-\sin\varphi}\right) \tag{9}$$

for $-54.8°\leqslant\varphi-n\,180°\leqslant 54.8°$ $(n=0,1,2\cdots)$ and

$$V_O=0.217\sqrt{2}\,|V_I|\begin{cases}\sqrt{1+\sin\varphi}, \\ -\sqrt{1-\sin\varphi},\end{cases}$$
$$\text{for}\quad \begin{matrix}-35.2°\leqslant\varphi-(4n+1)90°\leqslant 35.2°\\ -35.2°\leqslant\varphi-(4n-1)90°\leqslant 35.2°.\end{matrix} \tag{10}$$

The flat top of this response (Fig. 1(c)) is in practice only observed if one approaches ideal peak detection which can be the case, for instance, with high-level input signals.

If one input signal is large compared to the other signal, again a sinusoidal response is achieved. In the case where $|V_{I2}|\gg|V_{I1}|$, for instance, (9) and (10) reduce to

$$V_O=\frac{2}{\pi}|V_{I1}|\sin\varphi. \tag{11}$$

Thus also for a large input-level difference, circuit (c) delivers a lower output voltage than circuit (b).

In circuits (c) and (b) of Fig. 1, 90° hybrids are used. However, 180° hybrids can also be employed. Then the output characteristic is simply obtained by replacing $\sin\varphi$ in the above equations by $\cos\varphi$.

The circuits described above represent the simplest arrangements for phase detectors. More complicated circuits with four diodes, as used for double-balanced mixers, can also serve as phase detectors. However, in general, they have no advantage over the simple ones.

Since phase detection is based on peak detection, there is no need for a high-level signal to turn on the diodes as it is the case with the local-oscillator signal in a mixer. On the contrary, for reasons to be discussed later, it is advantageous to operate phase detectors with equal signal levels.

III. Large-Signal Analysis

The analytical expressions for the phase-detector characteristics in Section II have been derived assuming ideal circuits, matched diodes, and ideal peak detection. In practice, however, considerable deviation from these assumptions may occur. For instance, at low input level, the rectification can be far from peak detection because of the diode threshold voltage. Other effects which prevent ideal peak detection are the finite forward current, the parasitic elements of the package, and the finite load resistance.

Whereas real circuit parameters and diode mismatch can be considered by extending the analytical expressions of Section II, the real rectification process in the diodes can be only treated with a large-signal nonlinear analysis. Therefore, the following large-signal analysis has been applied allowing, in particular, consideration of real and different diode characteristics.

The Schottky-barrier diodes used are characterized by the equivalent circuit illustrated in Fig. 3. L_P, C_P, and L_B represent the diode package including the bond wires, whereas the diode chip is described by a series resistor R_S, a junction capacitance C_J, and a barrier resistance R_B. The voltage dependence of R_B is expressed by the well-known current–voltage relationship

$$i = i_s[\exp(\alpha v) - 1]. \tag{12}$$

The saturation current i_s and the slope factor of the current α are determined from the v–i curve of the actual diodes measured at dc. For the remaining elements, data given by the diode manufacturers have been used. The data used in the analysis are listed in Table I and apply to a micro-pill package.

The voltage dependence of the junction capacitance C_J, is neglected since it has only minor influence on the detector characteristic. However, the method of analysis described here is not restricted to one nonlinear element. It can be easily extended to consider the voltage dependence of the junction capacitance and the series resistance as well.

In order to solve the nonlinear problem, the phase detector equivalent circuit of Fig. 4(a) is divided into a linear and a nonlinear part (Fig. 4(b)). The linear part consists of the coupling network, which includes, e.g., a 3-dB hybrid and transmission lines, the internal impedances of the signal sources, and all voltage-independent elements of the diode equivalent circuits. For convenience, the voltage sources e_3 and e_4 are substituted by the corresponding current sources i_3 and i_4. With the simplified

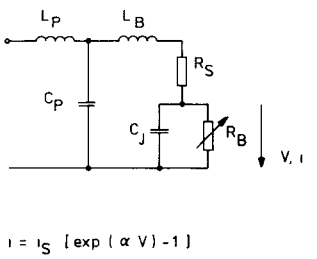

Fig. 3. Simplified equivalent circuit of a packaged Schottky-barrier diode.

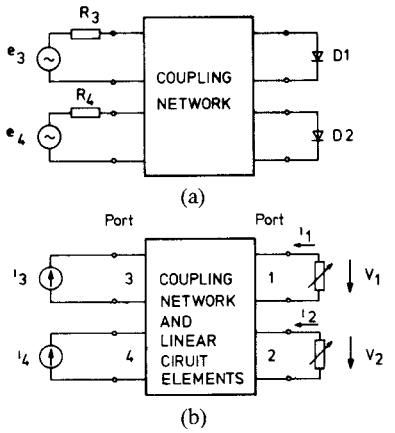

Fig. 4. Equivalent circuit of phase detector. (a) General circuit configuration. (b) Schematic for large-signal analysis.

TABLE I
Diode Data

DIODE TYPE		A	B
PACKAGE INDUCTANCE	L_P	0.2nH	0.2nH
PACKAGE CAPACITANCE	C_P	0.14pF	0.14pF
BOND WIRE INDUCTANCE	L_B	0.31nH	0.31nH
SERIES RESISTANCE	R_S	10 ohm	7 ohm
JUNCTION CAPACITANCE	C_J	0.1 pF	0.35pF
SATURATION CURRENT	I_S	6.76nA	71μA
SLOPE FACTOR	α	32/V	32/V

diode equivalent circuit of Fig. 3, the nonlinear part consists only of the two diode barrier resistances.

While the linear circuit part is most easily described in the frequency domain, the nonlinear part is more conveniently considered in the time domain. Thus the diode currents indicated in Fig. 4(b) are expressed as

$$i_m(t) = -i_{ms}[\exp(\alpha_m v_m(t) - 1], \qquad m = 1,2. \tag{13}$$

The remaining linear circuit can be characterized for one frequency by its impedance matrix $\boldsymbol{Z}$. However, the linear circuit is driven by a harmonic spectrum with frequencies $k\omega$ generated in the nonlinear part by the signal frequency ω. Thus k impedance matrices $\boldsymbol{Z}_k$ have to be determined according to the number of harmonics considered in the analysis. For the matrix elements z_{mnk}, explicit equations could be derived, however, it is more convenient to determine the elements with the aid of a computer program. Since the voltages at ports 3 and 4 are of no interest, only

the matrix elements z_{mnk} with $m=1,2$ have to be computed.

The voltages $v_m(t)$ and the currents $i_m(t)$ at ports 1 and 2 can be expressed in terms of Fourier coefficients as

$$v_m(t)=\sum_{k=-\infty}^{\infty} V_{mk}e^{jk\omega t}, \qquad V_{mk}=V_{m-k}^{*} \tag{14}$$

$$i_m(t)=\sum_{k=-\infty}^{\infty} I_{mk}e^{jk\omega t}, \qquad I_{mk}=I_{m-k}^{*} \tag{15}$$

where m indicates the ports and $k=0,\pm 1,\pm 2,\cdots$ the harmonics of the input frequency ω.

While $v_m(t)$ and $i_m(t)$ for $m=1,2$ are related by (13), the relationship between the Fourier coefficients V_{mk} and I_{mk} is given by the $\boldsymbol{Z}_k$ matrices as

$$\boldsymbol{V}_k=\boldsymbol{Z}_k\boldsymbol{I}_k. \tag{16}$$

For example, V_{1k} is obtained from (16) as

$$V_{1k}=z_{11k}I_{1k}+z_{12k}I_{2k}+z_{13}I_{3k}+z_{14k}I_{4k}. \tag{17}$$

The Fourier coefficients I_{1K} and I_{2K} are calculated from the currents $i_1(t)$ and $i_2(t)$, by

$$I_{mk}=\frac{1}{2\pi}\int_0^{2\pi} i_m(t)e^{-jk\omega t}d(\omega t). \tag{18}$$

I_{3k} and I_{4k} represent the currents impressed by the input signals. In the case of sinusoidal input signals, which is considered here, $I_{3k}=I_{4k}=0$ for $k\neq\pm 1$.

The desired output voltage V_O of the phase detectors is determined from the dc components of (18) I_{10} and I_{20}. With the load resistances indicated in Fig. 1 one obtaines

$$V_O=-I_{10}R_1+I_{20}R_2 \tag{19}$$

for circuit (b); and

$$V_O=(-I_{10}+I_{20})R \tag{20}$$

for circuit (c).

The solution of the problem is now found by matching the Fourier coefficients of the voltages at the boundaries between the linear and the nonlinear circuit part, that means at ports 1 and 2. The matching is performed in an iterative process, starting with an assumed set of coefficients V_{mk}. Using (14) and (13), one obtains the currents $i_m(t)$ from which the Fourier coefficients I_{mk} are calculated by (18).

Substituting these coefficients in (16) delivers the Fourier coefficients V_{mk} which are then compared with th initial values. The improved values for V_{mk} are calculat from the difference between the initial values and the new ones using special weighting factors to force rapid convergence. The computation is repeated until the differences between the coefficients V_{mk} of step n and $n+1$ vanish.

The convergence depends on the circuit elements, particularly on the diode current–voltage characteristic, and on the number of harmonics k taken into account. It was found that higher harmonics than $k=2$ are so small that they have only little influence on the detector characteristic. Therefore, the computations were performed with $|k|\leqslant 3$ where rapid convergence could be achieved.

Results obtained with the nonlinear analysis described here are given in the following sections. A comparison with measured detector characteristics (Figs. 8 and 9) demonstrates that this analysis allows accurate prediction of phase-detector performance.

IV. Sources of Characteristic Deformation

Before considering deviations from the ideal, let us define the ideal response. We call a phase-detector characteristic ideal if it is symmetrical to its zero crossings and its maxima and minima, respectively. Apart from this, the shape is not considered since even in an ideal circuit it depends on the element values and the input levels, particularly on the level difference.

In PSK demodulators, where the phase detectors are followed by hard limiting amplifiers, the shape of the detector characteristic has minor influence on the demodulator performance. Equidistant zero crossings are important to obtain low bit error rates. However, the effects which deform the shape of the characteristic in general also cause an unequal zero crossing shift.

As will be shown in the following, a deformation of the characteristic results either from circuit or diode imbalance.

A. Circuit Imbalance

In practice, circuit imbalance will be mainly caused by the input coupler. Due to imperfect dimensions and undesired stray fields, for instance, a 3-dB coupler shows finite isolation between the input ports, nonuniform power splitting, and nonideal phase shift. In general, these effects are not independent of each other. However, for simplicity, let us consider their influence on the detector characteristic separately.

The effects of circuit imbalance can be studied by modifying (3). Typical results obtained are shown in Fig. 5, and are discussed below.

1) Finite Isolation: The effect of finite isolation between the input signals on the detector characteristic can be easily understood from the vector diagram shown in Fig. 6. Both input voltages are mutually varied resulting in effective voltages which differ in phase and amplitude from the original ones.

Depending on the phase angles of the error vectors E_{12} and E_{21}, the detector characteristic can become asymmetrical with respect to the zero crossings and to the maxima (curves *b* and *c*, respectively, in Fig. 5). It is apparent from Fig. 6 that the characteristic deformation increases with the level difference of the input signals.

2) Nonuniform Power Splitting: In case of amplitude imbalance, the detector characteristic remains symmetrical with respect to the maxima but not to the zero crossings (curve *b*, Fig. 5). By shifting the characteristic with an external offset voltage one can obtain equidistant zero crossings, however, the response is still asymmetrical. For equal input levels, no asymmetry occurs if the couplers amplitude imbalance is the same for both signals.

3) Nonideal Phase Shift: In an imperfect hybrid coupler, the phase difference between the output signals may differ

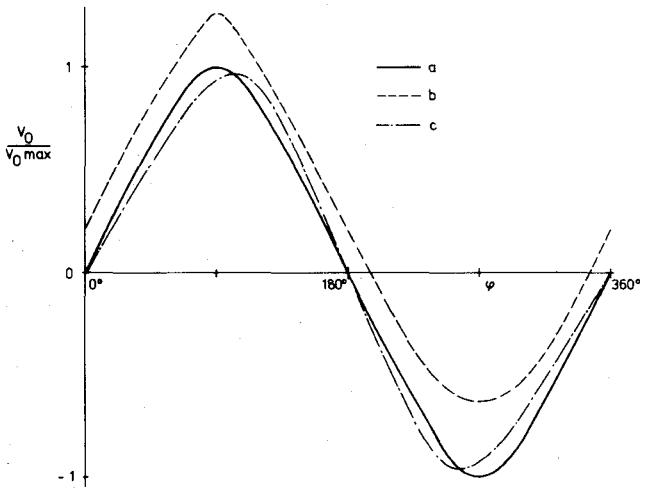

Fig. 5. Ideal detector characteristic (a) and typical deviations (b, c).

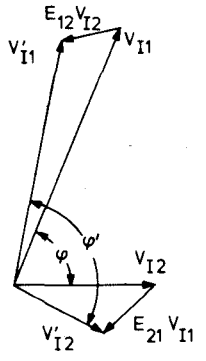

Fig. 6. Vector diagram showing the effect of interfering input signals. Phase deviation: $\Delta\varphi=\varphi'-\varphi$.

from the ideal value of 90°. Such a deviation causes the maxima and minima to shift but the characteristic remains symmetrical to the zero crossings (curve c, Fig. 5). Since the zero crossings are not affected, phase imbalance in the phase detector has virtually no effect on the performance of a PSK demodulator.

B. Diode Imbalance

Variation of the diode data may be caused by different packaging or different chip performances. Whereas packaging influences only the reflection coefficient, the voltage–current relationship affects both the reflection coefficient and the rectification process. In the following subsection, we consider these effects separately according to their origins.

1) Different Reflection Coefficients: For a diode with the reflection coefficient Γ_D, the voltage V_D of the incident wave is changed to

$$V_D'=V_D(1+\Gamma_D). \tag{21}$$

Depending on the phase angle of Γ_D the diode voltage is increased or decreased by reflection.

It is obvious that for equal reflection coefficients $\Gamma_{D1}=\Gamma_{D2}$ signal reflection does not alter the shape of the detector response but scales it up or down. In practice, however, the reflection coefficients depend on the diode voltages which vary with the phase difference between a maximum and a minimum value as shown in Fig. 2. If the reflection coefficients have the same voltage dependence $\Gamma_{D1}(V_{D1})=\Gamma_{D2}(V_{D2})$ the shape is changed but the characteristic remains ideal.

Different reflection coefficients result in an asymmetry with respect to the zero crossings (curve b, Fig. 5).

2) Different Voltage–Current Characteristics: The effect of different voltage–current characteristics can be completely described only with the nonlinear analysis of Section III. Fig. 7 shows results obtained with that analysis for unlike zero-bias diodes in the circuit arrangement of Fig. 1(b). The diodes are assumed to differ in their active chip area by 65 percent, which implies a corresponding difference in i_s, R_s, and C_J. This difference leads to a detector characteristic asymmetrical with respect to its zero crossings. The zero crossings shift is, however, almost independent of input-level variation. A similar performance degradation to that shown in Fig. 7 takes place if the voltage–current characteristics undergo relative changes to each other with temperature. It should be noted, however, that no zero crossing shift occurs if the temperature depen-

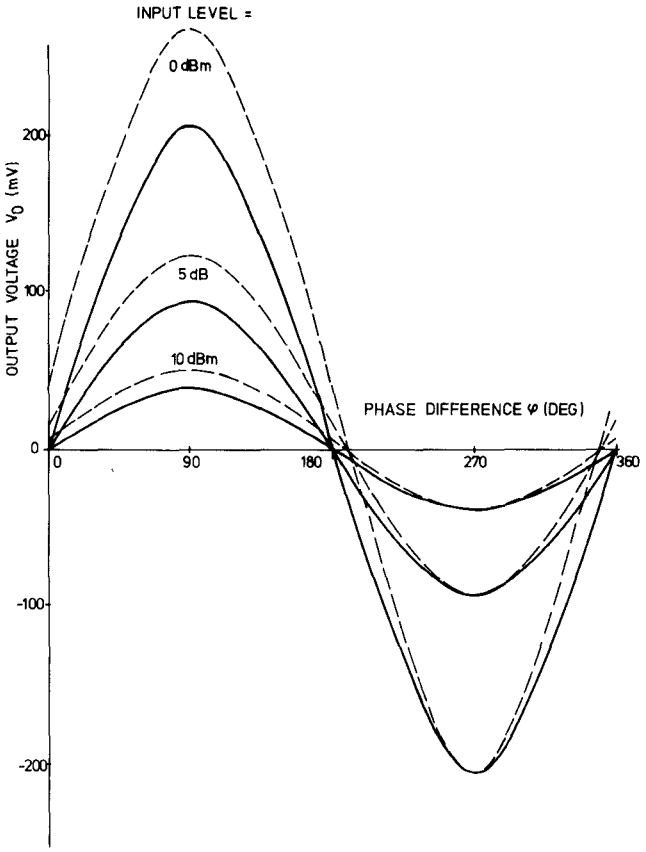

Fig. 7. Computed output characteristic of a phase detector with zero-bias Schottky diodes of equal and different chip area, respectively. Circuit of Fig. 1(b), $R_1 = R_2 = 250\ \Omega$, equal input levels. $p_{I1} = p_{I2} = p_I$, $f = 14.25$ GHz. —— : equal diodes. ---: chip area of diode 1 is 65 percent of the chip area of diode 2.

dence of the voltage–current characteristic is the same for both diodes.

V. Performance of Practical Circuits

The phase detectors described in this section have been built to demonstrate their suitability for use in a differential PSK demodulator which is to be used in a regenerative satellite repeater. The design goals for the demodulator, and thus for the phase detectors, were: low input power, high dynamic range, and high phase accuracy. The circuits have been realized in microstrip technique with 3-dB ring hybrids, and cover the satellite band from 14.0 to 14.5 GHz.

Fig. 8 shows the output characteristic of a phase detector with low-barrier silicon Schottky diodes connected together at one side (circuit in Fig. 1(c)). The measured curves are in good agreement with the theoretical ones obtained with the nonlinear analysis of Section III. The zero crossings are equidistant and show virtually no shift with input-level variation from 10 to 0 dBm. At lower and higher input level, the phase error, that is the deviation of the zero crossings from the ideal values, exceeds 2°. In order to achieve lower input-level operation, zero-bias Schottky diodes with vanishing threshold voltage have been inserted.

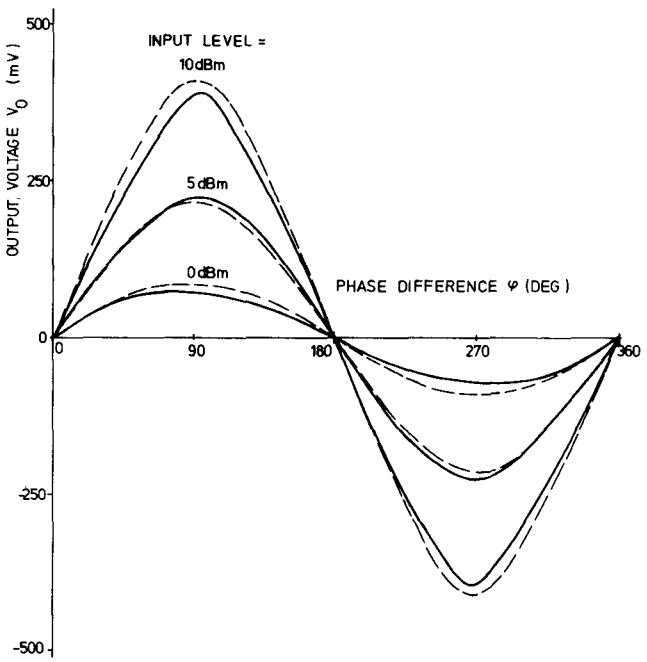

Fig. 8. Measured and computed output characteristic of a phase detector with low-barrier Schottky diodes. Circuit of Fig. 1(c), $R = 50\ \Omega$, equal input levels $p_{I1} = p_{I2} = p_I$, $f = 14.25$ GHz. —— : measured. ---: computed.

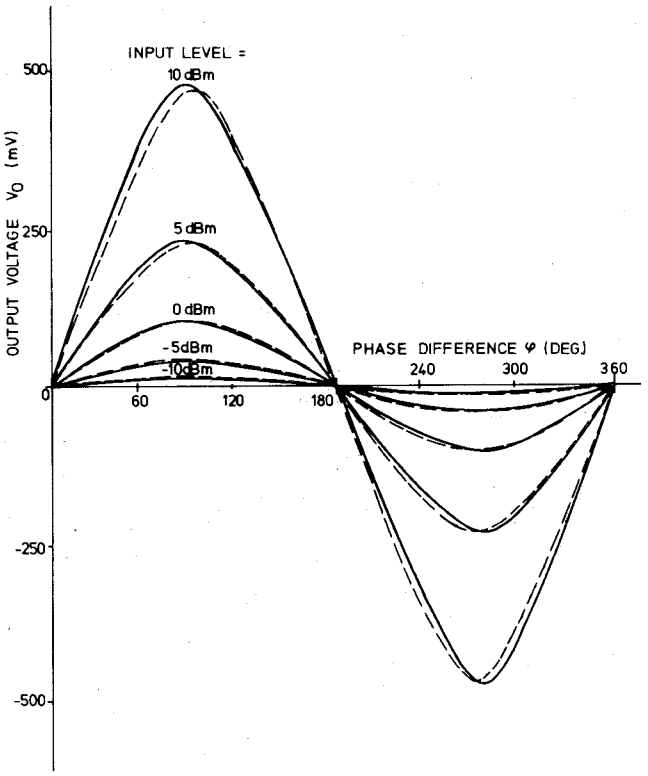

Fig. 9. Measured and computed output characteristic of a phase detector with zero-bias Schottky diodes. Circuit of Fig. 1(b), $R_1=50\ \Omega$, $R_2=48.6\ \Omega$, equal input levels $p_{I1}=p_{I2}=p_I$, $f=14.25$ GHz. —— : measured; ---: computed.

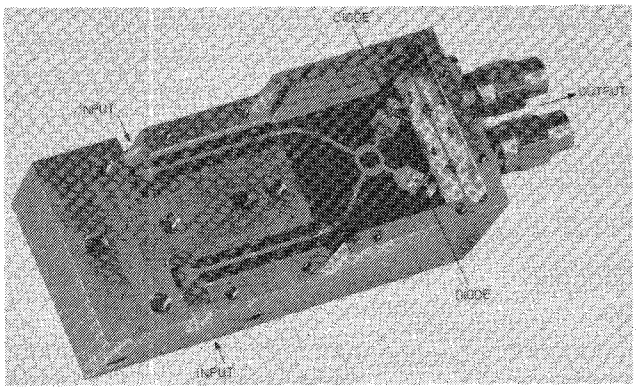

Fig. 10. Phase detector on fused silica substrate for the 14.0–14.5-GHz band with matched zero-bias Schottky diodes.

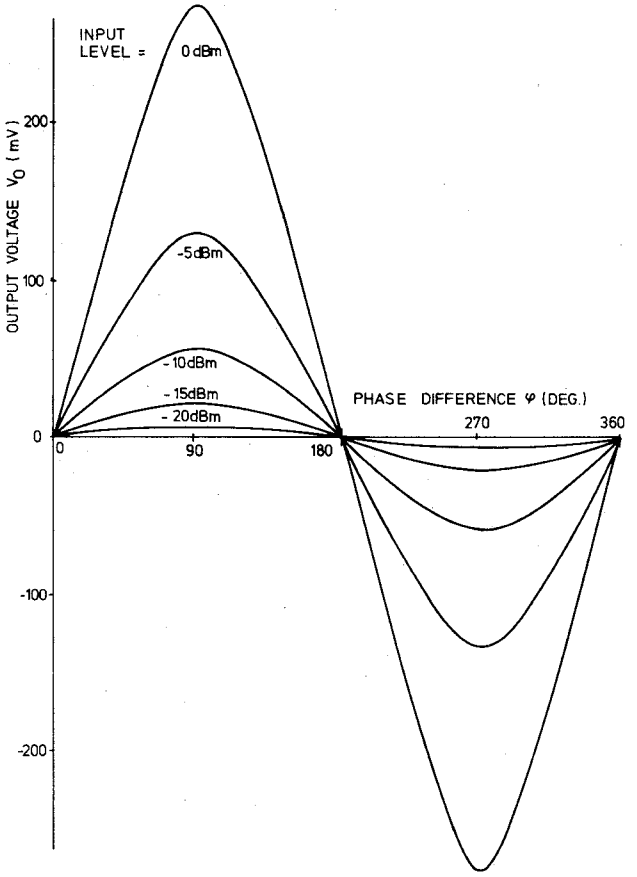

Fig. 11. Measured output characteristic of the phase detector of Fig. 10 with matched zero-bias Schottky diodes. Circuit of Fig. 1(b), $R_1=250\ \Omega$, $R_2=205\ \Omega$, equal input levels $p_{I1}=p_{I2}=p_I$, $f=14.25$ GHz.

However, due to the large variation in the current–voltage characteristics, which is typical for these diodes, phase errors of more than 10° occurred. Zero-bias diodes are thus not suitable for phase detectors with the circuit arrangement of Fig. 1(c).

In the detector circuit of Fig. 1(b), the imbalance of the diode characteristics and in the circuit can be compensated by means of the output resistances R_1 and R_2. Selecting different values for R_1 and R_2 one can easily shift the zero crossings. Fig. 9 shows the output characteristic of a phase detector (circuit of Fig. 1(b)) with silicon zero-bias Schottky diodes. The measured curves are in excellent agreement with the calculated ones. Equidistant zero crossings are obtained by choosing slightly different output resistances. The phase error remains below 2° for 20-dB level variation. At −10-dBm input level, the detector still delivers sufficient output voltage with low phase error.

The detector sensivity can be further increased by matching the diodes and utilizing higher output resistances. Fig. 10 shows a photograph of a phase detector (circuit of Fig. 1(b)) with matched zero-bias diodes, realized on a fused silica substrate. Its measured output characteristic for 250-Ω load resistances is plotted in Fig. 11. The detector operates down to −20-dBm input level with high phase accuracy. For level variation from 0 to −20 dBm, the phase error does not exceed 2°. In the level range from 0 to −10 dBm, the phase error remains below 1° at room temperature, and below 2° for temperatures between 10 and 40°C. Varying the frequency from 14.0 to 14.5 GHz, an additional phase error of 2° occurs. However, at any frequency within that band, the phase detector can be adjusted to zero phase error for a given input level. The adjustment is simply performed by varying the load resistances. The return loss in the 500-MHz band is higher than 20 dB.

Fig. 12 gives a comparison between the measured output voltages of the phase detectors with the characteristics shown in Figs. 8 and 11, respectively. The maximum

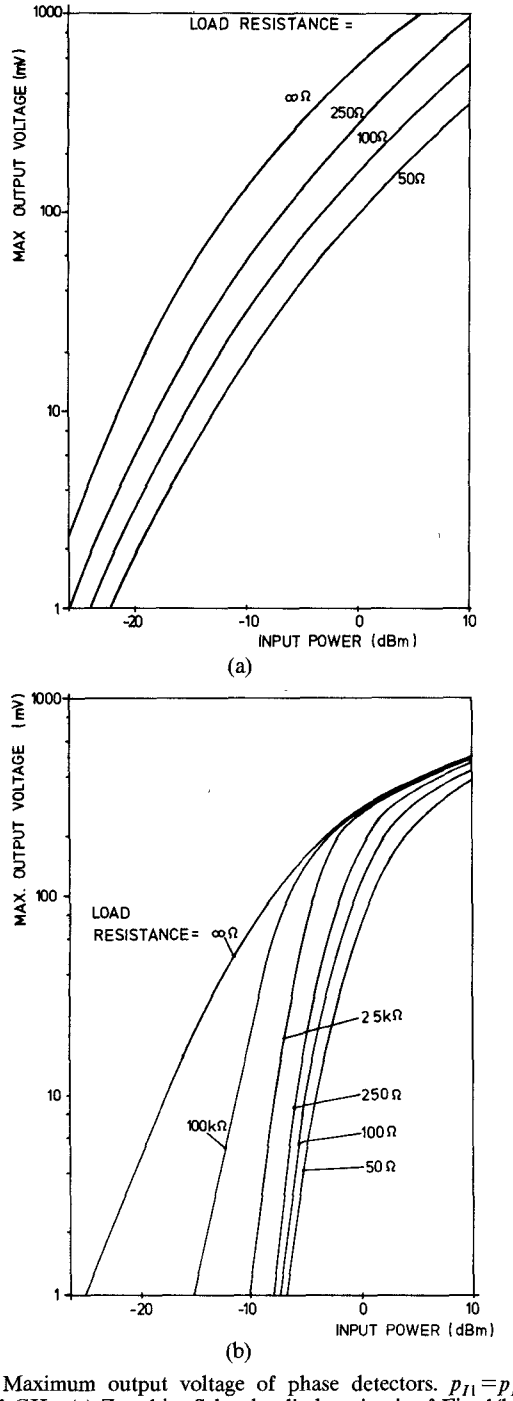

Fig. 12. Maximum output voltage of phase detectors. $p_{I1}=p_{I2}=p_I$, $f=14.25$ GHz. (a) Zero-bias Schottky diodes, circuit of Fig. 1(b), (Fig. 11). (b) Low-barrier Schottky diodes, circuit of Fig. 1(c), (Fig. 8).

output voltages are plotted against the input power for different load resistances. This comparison demonstrates the higher output efficiency of the phase detector with separate diodes. It should be mentioned, however, that the essentially higher output voltage at low levels is mainly due to the use of zero-bias diodes.

Besides higher sensivity and the possibility of imbalance compensation, the phase detector with separate diodes has the advantage of a symmetrical output. This is of particular importance for PSK demodulators, since it allows direct connection to the following dc-coupled differential amplifier.

VI. Conclusion and Summary

The simplest circuits for microwave phase detection and their principles of operation have been described. Approximate analytical expressions for the output characteristic of various phase detectors could be derived allowing comparision of their fundamental features. Exact prediction of phase-detector performance with a large-signal nonlinear analysis has been demonstrated. For the analysis, the circuit has been divided into a linear part treated in the frequency domain and a nonlinear part treated in the time domain.

With the aid of the theory developed all effects that may cause deformation of the detector characteristic have been covered. It has been shown that characteristic deformation results either from circuit or diode imbalance, and that minimum distortion is achieved for equal input levels.

The performances of practical circuits have been compared with respect to their implementation in PSK demodulators. The single-balanced arrangement with separate diodes was found to be best suited. It has been demonstrated how accurate phase detectors, which operate at low input levels with a high dynamic range, can be built.

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